WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
an input pin row including a plurality of input pins;
an output pin row including a plurality of output pins;
a memory cell array including a plurality of cell plates in a plurality of cell columns between the input and output pin rows;
a plurality of sense amplifiers in two amplifier columns disposed between the adjacent two of the plurality of cell columns;
an address circuitry;
an address transition detector (ATD) circuitry to provide an ATD pulse upon detecting a transition in the address circuitry;
an ATD pulse synthesizer to provide a synthesized pulse in response to the ATD pulse;
an output circuitry; and
a delay circuitry to provide a sense amplifier data latch signal and an output data latch signal in response to the synthesized pulse from the ATD pulse synthesizer,
at least the address, ATD and delay circuitries being disposed between the input pin row and the plurality of cell columns,
the ATD pulse synthesizer being disposed between the two amplifier columns and spaced a predetermined signal transmission path from the ATD and delay circuitries.

2. The semiconductor memory device as claimed in claim 1, further comprising:
an error correction code (ECC) circuitry disposed

between the two amplifier columns together with the ATD pulse synthesizer, and the delay circuitry provides an ECC data latch signal.

3. The semiconductor memory device as claimed in claim 1 or 2, wherein said output circuitry is disposed between the two amplifier columns and between the ATD pulse synthesizer and the output pin row.

4. The semiconductor memory device as claimed in claim 1 or 2, wherein said output circuitry is disposed between the cell columns and the output pin row.

5. The semiconductor memory device as claimed in claim 1 or 2, wherein the device has write function.

6. The semiconductor memory device as claimed in claim 1 or 2, wherein the address, ATD and delay circuitries only are disposed in a site between the input pin row and the plurality of cell columns.

7. The semiconductor memory device as claimed in claim 1 or 2, wherein the number of the plurality of cell plates is four.

8. The semiconductor memory device as claimed in claim 1 or 2, wherein the output pin row includes at least one input pin.

9. The semiconductor memory device as claimed in claim 1 or 2,

wherein each of the plurality of cell columns include a plurality pairs of cell plates, and

further comprising:

a plurality of X-decoders, each disposed between the cell plates of one of the plurality of pairs;

a plurality of Y-select circuits, each disposed between an inner side of the cell plates of one of the plurality of pairs and the adjacent sense amplifier of one of the amplifier columns; and

a plurality of X-predecoders, each disposed adjacent an outer side of the cell plates of one of the plurality of pairs.

10. The semiconductor memory device as claimed in claim 1 or 2, wherein the memory cell array includes a plurality of horizontal digit lines, and a plurality of vertical word lines.